

# *K1GE*

# *Technical*

# *Reference*

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**FOR GENERAL DEVELOPMENT**

## Revision History

Ver	Date	Revision	In Charge	Requested
1.00		Initial	Yokoyama	-
1.01	1998.02.27	General Development	Takeda	-
1.02	1998.05.18	1. Grammatical Correction 2. Explanation for Clear Color Added 3. Operation Timing Added	Takeda	-

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## 1. FEATURES

1. DOUBLE LINE BUFFER METHOD
2. CHARACTER RAM METHOD
3. SCROLL AND SPRITE USE COMMON CIRCUIT
4. SCROLL VRAM, SPRITE VRAM, CHARACTER RAM COMMON
5. ALL RAM INTERNAL
6. LUT INTERNAL, COLOR LEVEL CHANGE BY USE OF PALETTE LUT
7. LCD INTERFACE INTERNAL

## 2. DISPLAY SPECIFICATION

SCREEN SIZE	160[dot]×152[dot] <sup>1</sup>
COLOR LEVEL	8 LEVELS
FRAME RATE	60[F/S] <sup>2</sup>
INTERFACE	LCD INTERFACE
SPRITE CONTROLLER	CAPABLE OF DISPLAYING 64 8[dot] × 8[dot] CHARACTERS
SCROLL CONTROLLER	CAPABLE OF DISPLAYING 2 SCROLLABLE BACKGROUND

### 2-1. COORDINATES AND DISPLAY AREA

VIRTUAL DISPLAY AREA	256[dot] × 256[dot] CYCLICAL STRUCTURE
ACTUAL DISPLAY AREA	160[dot] × 152[dot]

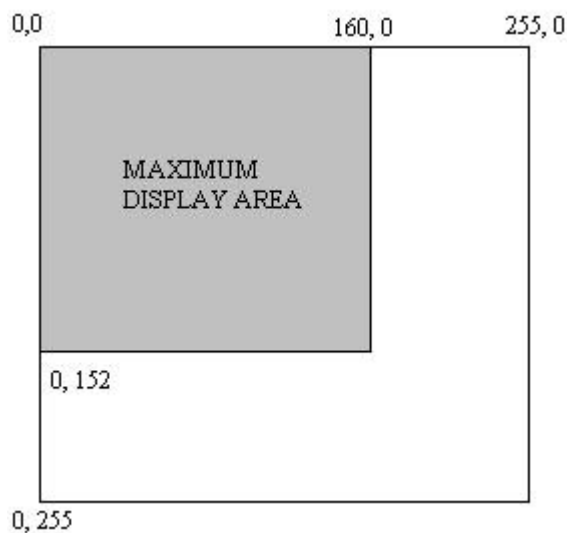


FIGURE 1. WORLD COORDINATES AND DISPLAY AREA

<sup>1</sup> DOT ASPECT IS ALWAYS 1:1

<sup>2</sup> CHANGABLE

### 3. GRAPHIC ENGINE

GRAPHIC ENGINE<sup>3</sup> is similar to other systems. In order to decrease the necessary circuitry, sprite display and scroll display use a common circuitry. There are no special cautions that need to be followed when programming.

#### 3-1. MEMORY LAYOUT

All three memory types of K1GE (character RAM, VRAM, and line buffer) are included in the ASIC. Of these, the character RAM and VRAM are under CPU control and are common with the scroll control. The layout and amount of memory is as follows.

<i>Character RAM</i>	
Size	: 8KB
Layout	: $512 \times \{(8 \times 8) \times 2\} = 65.536\text{Kb} = 8.192 \text{ KB}$ characters $\times \{(\text{dots vertically} \times \text{dots horizontally}) \times \text{levels}\}$
<i>VRAM</i>	
Size	: 4.25KB
Layout	: $1024 \times 16 \times 2 = 32.768\text{Kb} = 4.096\text{KB}$ (scroll control only) maximum characters(1 screen) definable in RAM x parameters necessary to describe 1 character x scrollable plane numbers $64 \times 32 = 2.048\text{Kb} = 256\text{Bytes}$ (sprite control only) maximum characters(1 screen) definable in RAM x parameters necessary to describe 1 character
<i>Line Buffer</i>	
Size	: 256B
Layout	: $\{(4 \times 16) \times 16\} \times 2 = 2.048\text{Kb} = 256\text{Bytes}$ (to transfer 8 dots simultaneously) x double buffer

#### 3-2. MEMORY MAP

0X8000	Control Registers	There is an open area in the address register. PLEASE DO NOT ACCESS. (Future expansion)
0X87FF		
0X8800		
0X88FF	Sprite VRAM	PLEASE DO NOT ACCESS. (Future expansion).
0X8900	vacant	
0X8FFF		
0X9000	Scroll VRAM	
0X9FFF		
0XA000	Character RAM	
0XBFFF		

Figure 2. K1GE Memory Map

<sup>3</sup> Graphics Engine will be designated as K1GE from this point onward

### 3-3. SPRITE CONTROL

#### 3-3-1. Specification for Sprite Control

# of sprites displayable in one frame	64
# of sprites displayable in one line	64 <sup>4</sup>
maximum characters definable in VRAM	64
maximum character definable	512 characters <sup>5</sup>
levels available	8 levels <sup>6</sup>
character size	8[dot] × 8[dot] fixed

#### 3-3-2. Display Function for Sprite Control

function available to whole screen	Position correction function
function available to each sprite	Flip function
	Defining priority with scroll screen
	Character position chain function

#### 3-3-3. Data Format for Sprite VRAM

VRAM data format is as follows.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0X8800	<i>C.C(8+1Bit)</i>							
0X8801	<i>H.F</i>	<i>V.F</i>	<i>P.C</i>	<i>PR.C</i>		<i>H.ch</i>	<i>V.ch</i>	<i>C.C</i>
0X8802	<i>H.P(8Bit)</i>							
0X8803	<i>V.P(8Bit)</i>							

\*Start address for VRAM is 0X8800. The above example shows the first set of parameters, 4 bytes each. Since there are memory space for 64 sprites, there are 256 bytes available.

**Table 1. Parameters and Definitions**

<b>V.P</b>	
V position	Y coordinate for the character.
<b>H.P</b>	
H position	X coordinate for the character.
<b>C.C</b>	
Character code	Setting character code.
<b>H.F</b>	
H Flip	Character display status.

(Continued)

<sup>4</sup> Except, there is a possibility of “character over.” Explanation on page 18.

<sup>5</sup> Common with scroll character.

<sup>6</sup> 8 levels of gray excluding clear. Only 4 levels maybe used in one character (clear would be counted as well).

(Continuation)

V.F		
V Flip	Character display status.	
	V.F Logic	Display status
	0	Normal
	1	Vertically Mirrored
P.C		
Palette Code	Specifies palette code.	
PR.C		
Priority Code	Priority level with respect to scroll screen.	
	Value of PR.C	Priority
	00	Character not shown
	01	Furthest
	10	Middle
	11	Front
H.ch		
H Position Chain	Value defined becomes the offset value with respect to the previous character.	
	H.ch Logic	Display status
	0	Normal Coordinates
	1	Offset Coordinates
V.ch		
V Position Chain	Value defined becomes the offset value with respect to the previous character.	
	V.ch Logic	Display status
	0	Normal Coordinates
	1	Offset Coordinates
D.C		
Do not care	This register value has no effect.	

### 3-3-3-1. VRAM Address and Character Sprite Priority

Priority for sprites on screen is dependent on the VRAM address. The hardware reads the values from the VRAM 0 address and writes to the line buffer. During the write to the line buffer, the hardware checks the priority as follows to avoid writing over previously written data.

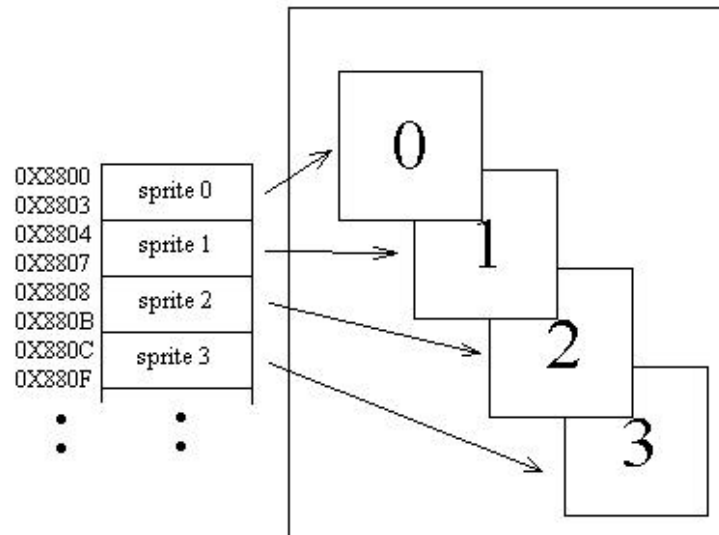


Figure 3. Scroll Screen and Sprite Priority Relation

### 3-3-3-2. Scroll Screen and Sprite Priority

Figure 4 shows the P.R.C value and the priority.

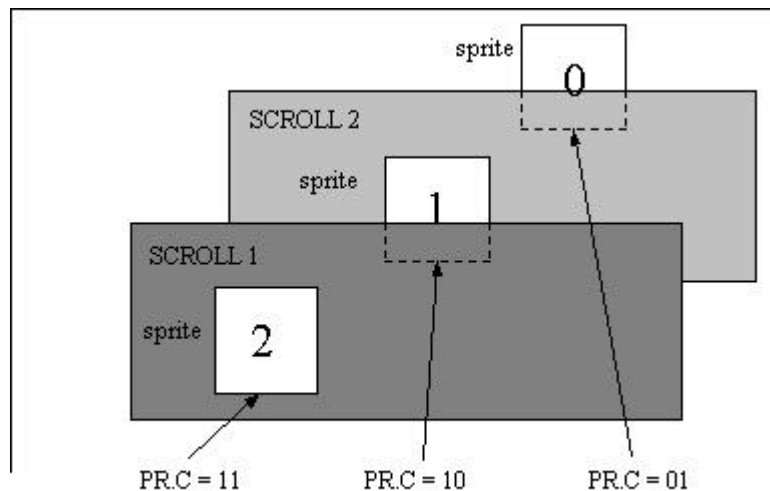


Figure 4. Scroll Screen and Sprite Priority Relationship



### 3-3-4. Sprite Position Offset Function

The value inside this register is added as an offset to the sprite position. The relationship between sprite position and offset is as follows:

$$H' = H + PO.H$$

$$V' = V + PO.V \text{ (over flow ignored)}$$

Because a value over 256 is ignored, overflow values are ignored and the value is set to 256. Since this value is always added to the sprite position, please initialize with 0X00 if offset is not required.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0X8020	PO.H(8Bit)							
0X8021	PO.V(8Bit)							

\*Caution: When the value in this register is set, it is reflected in the following line.

**Table 2. Parameters and Definitions**

PO.H	
H Position offset	Value to be added to the X value of the sprite. After reset, the initial value is 0X00.
PO.V	
V Position offset	Value to be added to the Y value of the sprite. After reset, the initial value is 0X00.

### 3-3-5. Data Format for Sprite Characters

Each dot in a sprite character has 4 levels. For CPU connection reasons, 1 byte is 1 address and thus 1 address has data for 4 dots<sup>7</sup>. Bits are positioned as in Figure 5. Address bus above A4 corresponds with the character code. The CPU data bus is 16 bit, but the format is in this fashion due to it being a “little-endian.”

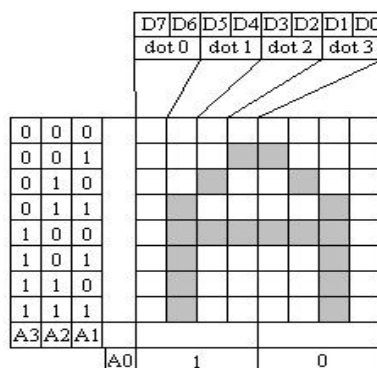


Figure 5. Sprite Character ROM Data Format

<sup>7</sup> For each dot, there are 2 bits information which determines the color (4 total including clear). Character color information is given in 3-7 palette LUT for sprites.

### 3-3-5-1. Relationship Between Sprite Character Data and Address

The relationship between character dot data and its address is as follows. The table below shows data and address for one character. 1 row of data represents 1 line on screen.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0XA000	<i>Dot 4</i>		<i>Dot 5</i>		<i>Dot 6</i>		<i>Dot 7</i>	
0XA001	<i>Dot 0</i>		<i>Dot 1</i>		<i>Dot 2</i>		<i>Dot 3</i>	
0XA002	<i>Dot 4</i>		<i>Dot 5</i>		<i>Dot 6</i>		<i>Dot 7</i>	
0XA003	<i>Dot 0</i>		<i>Dot 1</i>		<i>Dot 2</i>		<i>Dot 3</i>	
0XBFFC	<i>Dot 4</i>		<i>Dot 5</i>		<i>Dot 6</i>		<i>Dot 7</i>	
0XBFFD	<i>Dot 0</i>		<i>Dot 1</i>		<i>Dot 2</i>		<i>Dot 3</i>	
0XBFFE	<i>Dot 4</i>		<i>Dot 5</i>		<i>Dot 6</i>		<i>Dot 7</i>	
0XBFFF	<i>Dot 0</i>		<i>Dot 1</i>		<i>Dot 2</i>		<i>Dot 3</i>	

### 3-4. SCROLL CONTROL

#### 3-4-1. Specification for Scroll Control

Scrollable planes	2 planes
Virtual screen size	256[dot] x 256[dot]
Maximum VRAM definable characters	2048 <sup>8</sup> characters
Maximum definable characters	512 <sup>9</sup> characters
Usable color levels	8 levels
Character size	8[dot] x 8[dot]fixed

#### 3-4-2. Display Function for Scroll Control

Function applicable to screen	Changing priority of scroll planes Window function <sup>10</sup>
	Changing frame rate
	Function to read raster position
	Screen control such as forced blanking
Function applicable to each character	Flip(mirroring) function
Other functions	Scan line interrupt(Hint)
	Frame interrupt(Vint)
	LCD duty control

#### 3-4-3. Relationship of VRAM Address and Scroll Plane

Figure 6 shows VRAM address and scroll plane relationship.

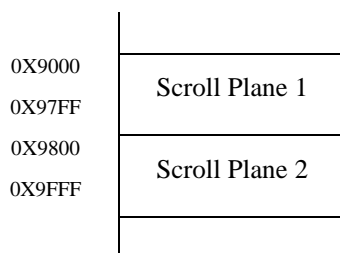


Figure 6. VRAM Address and Scroll Plane Relationship

#### 3-4-4. Interrupt Control Register

K1GE produces interrupts after drawing the screen<sup>11</sup> and before the line is drawn(beginning of a line)<sup>12</sup>. ON/OFF of interrupts are set in the interrupt control register. The format is as follows.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0X8000	<i>VI.E</i>	<i>HI.E</i>	<i>D.C</i>					

\* Caution: Register setting affects the system with no time delay (at once).

<sup>8</sup> 32character×32character×2planes.

<sup>9</sup> Common with sprite characters.

<sup>10</sup> Display area function.

<sup>11</sup> Called Vint.

<sup>12</sup> Called Hint.

**Table 3. Parameters and Definitions**

<b><i>V.I.E</i></b>		
Frame interrupt Permission	Controls ON/OFF of frame interrupt.	
	<b>V.I.E Logic</b>	<b>Operation</b>
	0	Interrupt not permitted: Frame interrupt is not permitted. Status after reset of system(initial).
	1	Interrupt permitted: Frame interrupt is permitted.
<b><i>H.I.E</i></b>		
Scan Line interrupt Permission	Controls ON/OFF of scan line interrupt.	
	<b>H.I.E Logic</b>	<b>Operation</b>
	0	Interrupt not permitted: Scan line interrupt is not permitted. Status after reset of system(initial).
	1	Interrupt permitted: Scan line interrupt is permitted.

### 3-4-5. Data Format for Scroll Plane VRAM

VRAM data format is as follows.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0X9000	<i>C.C(8+1Bit)</i>							
0X9001	<i>H.F</i>	<i>V.F</i>	<i>P.C</i>	<i>D.C</i>			<i>C.C</i>	

\* Start address of VRAM for scroll plane is 0X9000. Only one parameter group is shown above. Address increases 2 bytes when used.

**Table 4. Parameters and Definitions**

C.C		
Character Code	Sets character code. Character code is common with the sprites.	
H.F		
H Flip	Character display status.	
	H.F Logic	Display status
	0	Normal
	1	Horizontally mirrored
V.F		
V Flip	Character display status.	
	V.F Logic	Display status
	0	Normal
	1	Vertically mirrored
P.C		
Palette Code	Setting palette code.	
D.C		
Do not care.	This register value has no effect.	

### 3-4-6. VRAM Address and the Relationship to the Position on Screen

VRAM address and the positioning on screen with respect to each other are as follows:

0X9000	0X9002	0X9004		0X903E
0X9040	0X9042	0X9044		0X907E
0X97C0	0X97C2	0X97C4		0X97FE

Figure 7. VRAM Address and Screen Position Relationship

As can be seen, increasing the address moves the position horizontally. The second scroll plane address is from 0X9800 to 0X9FFE.

### 3-4-7. Priority Levels of Scroll Planes

Priority of scroll planes with respect to each other is as follows. Changing the value in the register switches the priority level.

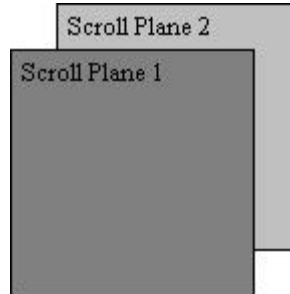


Figure 8. Scroll Plane Priority

### 3-4-8. Register to Change Priority Level of Scroll Planes

Changes the scroll plane priority level. Register value and priority is shown in Figure 9.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0X8030	<i>P.F</i>	<i>D.C</i>						

\*Caution:

This register setting affects takes effect from the next line being drawn.

**Table 5. Parameters and Definitions**

P.F							
Scroll Plane Priority Switching	Switches the priority level of scroll planes.						
	<table><tr><th>P.F Logic</th><th>Display Status</th></tr><tr><td>0</td><td>Normal: Scroll Plane 1 is in front. After system reset, this is the value (initial).</td></tr><tr><td>1</td><td>Switched: Scroll Plane 2 is in front.</td></tr></table>	P.F Logic	Display Status	0	Normal: Scroll Plane 1 is in front. After system reset, this is the value (initial).	1	Switched: Scroll Plane 2 is in front.
	P.F Logic	Display Status					
0	Normal: Scroll Plane 1 is in front. After system reset, this is the value (initial).						
1	Switched: Scroll Plane 2 is in front.						

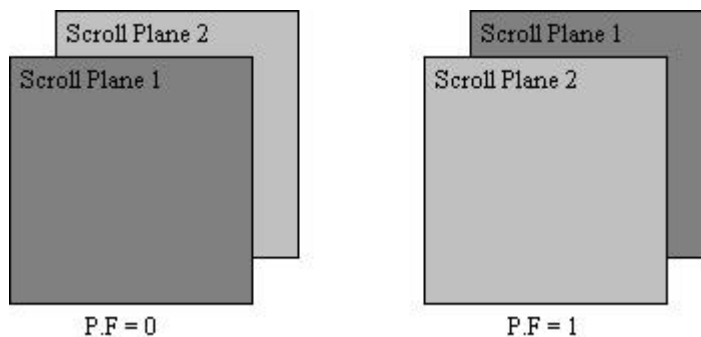


Figure 9. P.F Logic Value and Priority

### 3-4-9. Scroll Offset Register

Sets the scroll plane offset value. The relationship of the offset and display is shown in Figure 10.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0X8032	SISO.H(8Bit)							
0X8033	SISO.V(8Bit)							
0X8034	S2SO.H(8Bit)							
0X8035	S2SO.V(8Bit)							

\*Caution:

Register value affects the display from the line drawn after setting.

**Table 6. Parameters and Definitions**

<b>SISO.H</b>	
Scroll Plane 1 H Scroll Offset	Scroll Plane 1 X scroll offset. After system reset, 0x00(initial value).
<b>SISO.V</b>	
Scroll Plane 1 V Scroll Offset	Scroll Plane 1 Y scroll offset. After system reset, 0x00(initial value).
<b>S2SO.H</b>	
Scroll Plane 2 H Scroll Offset	Scroll Plane 2 X scroll offset. After system reset, 0x00(initial value).
<b>S2SO.V</b>	
Scroll Plane 2 V Scroll Offset	Scroll Plane 2 Y scroll offset. After system reset, 0x00(initial value).

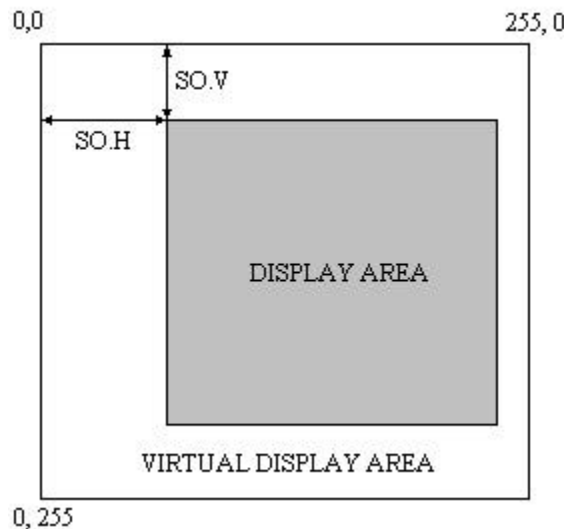


Figure 10. Scroll Offset and Display Area

### 3-4-10. Window Register

Determines the window display area. WBA.n is the windows origin, and WSI.n determines the window size. Non-display area is blank<sup>13</sup>. Figure 11 shows the register and screen relationship.

<sup>13</sup> Blank is set in 3 – 6 2D control 00WC.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0X8002	WBA.H(8Bit)							
0X8003	WBA.V(8Bit)							
0X8004	WSI.H(8Bit)							
0X8005	WSI.V(8Bit)							

\*Caution:

Since WBA.n and WSI.n determines the window position and size, the lower right corner of the widow may exceed the display area. When this occurs, the following operation is performed by the hardware. The register value takes effect from the next frame.

WBA.n and the Sum (WBA.n + WSI.n)	Operation
WBA.n value is outside the display area	Screen is blank
Sum of WBA.n and WSI.n is outside the display area	Only area inside the display area is valid

**Table 7. Parameters and Definitions**

<b>WBA.H</b>	
Window H origin	Sets the window origin X value. After system reset 0x00(initial value)
<b>WBA.V</b>	
Window V origin	Sets the window origin Y value. After system reset 0x00(initial value)
<b>WSI.H</b>	
Window H size	Sets the X size of window. After system reset 0xFF(initial value)
<b>WSI.V</b>	
Window V size	Sets the Y size of window. After system reset 0xFF(initial value)

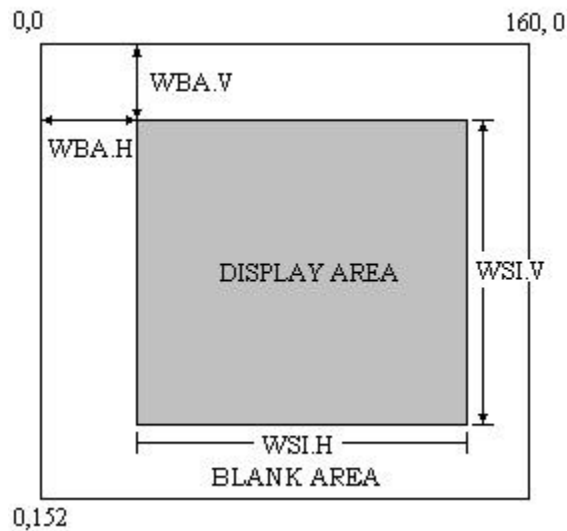


Figure 11. Display Area and Window Function Relationship



### 3-4-11. Relationship of Vint and Screen Setup

Care must be taken concerning interrupts which occur after the screen is drawn by the K1GE CPU, because the timing at which the interrupt occurs is dependent on the value in the Window Register. The end of drawing is dependent on the displayed area, and Vint occurs when the line WBA.V + WSI.V is drawn. The exception is when WSI.V = 0. Then Vint occurs when the line is at WBA.V.

### 3-4-12. Relationship of Hint and Screen Setup

Hint is different from Vint and is not dependent on the value set in the Window Register. It is constant and 152 Hint occur every time.

### 3-4-13. Raster Position Register

Reading the value in this register allows access to the current raster position.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0X8008	RAS.H(8Bit)							
0X8009	RAS.V(8Bit)							

\*Caution: LCD and Scan Line

Unlike a CRT, LCD does not have a scan line. In this case, the signal inside of the ASIC is used as the raster position.

Upper 8 bits of the 10 bit internal subtraction counter of the horizontal drawing operation time (internally 515 clock) is read in to RAS.H. (The value decreases as the horizontal drawing operation period progresses, and this value is accessible during V blank.)

RAS.V obtains the current line number during horizontal drawing operation. (Accessible during V blank.)

**Table 8. Parameters and Definitions**

RAS.H	
Raster position H	Remaining horizontal drawing operation time
RAS.V	
Raster position V	Horizontal drawing operation line number (Vertical Coordinate)

### 3-4-14. Scroll Character Data Format

The format is common with the sprites.

### 3-5. 2D STATUS REGISTER

This register is used to determine the internal status of K1GE.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0X8010	<i>C.OVR</i>	<i>BLNK</i>	<i>D.C</i>					

**Table 9. Parameter and Definitions**

<i>C.OVR</i>							
Character Over	Determines the character over status.						
	<table><tr><th>C.OVER Logic</th><th>Operation</th></tr><tr><td>0</td><td>Character Over has not occurred</td></tr><tr><td>1</td><td>Character Over has occurred: With the end of V blanking, it is cleared</td></tr></table>	C.OVER Logic	Operation	0	Character Over has not occurred	1	Character Over has occurred: With the end of V blanking, it is cleared
	C.OVER Logic	Operation					
0	Character Over has not occurred						
1	Character Over has occurred: With the end of V blanking, it is cleared						
<i>BLNK</i>							
Blanking	Determines if blanking or not						
	<table><tr><th>BLNK Logic</th><th>Operation</th></tr><tr><td>0</td><td>Displaying</td></tr><tr><td>1</td><td>V Blanking</td></tr></table>	BLNK Logic	Operation	0	Displaying	1	V Blanking
	BLNK Logic	Operation					
0	Displaying						
1	V Blanking						

\* Character Over is:

K1GE sprites<sup>14</sup> uses the line buffer method. Character Over is a phenomenon associated with a line buffer method sprite system. This phenomenon results from the system determining visibility of the sprite after reading in from the VRAM and then updating the line buffer. Due to an operation which results in this process not being completed in one scan line period, the character disappears partially or completely. This phenomenon is called Character Over, or Sprite Line Over<sup>15</sup>. Because the K1GE writes two scroll planes and sprites to the line buffer, processing time is limited. Normally Character Over will not occur, but if a program is written that accesses the VRAM frequently, Character Over may occur.

<sup>14</sup> Internally K1GE does not differentiate between sprites and scroll planes.

<sup>15</sup> As can be seen from previous comments, this phenomenon is referred to as Character Over in this documentation.

### 3-6. 2D CONTROL

This register sets the display setting and color setting for outside the window related to the LCD display.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0X8012	NEG							OOWC

\* Caution:

Setting in this register is reflected in the next line being drawn on screen.

**Table 10. Parameters and Definitions**

NEG	
Negative and Positive Switched	Negative and positive of the screen display is switched.
OOWC	
Outside window color	Color setting outside the window. After reset 0X0 (initial).

### 3-7. PALETTE LUT<sup>16</sup> FOR SPRITES

Palette code (P.C) defined in the sprite VRAM is changed to the value set in this register. Register format is as follows.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0X8100	Access not allowed.							
0X8101	D.C					SPPLT.01		
0X8102	D.C					SPPLT.02		
0X8103	D.C					SPPLT.03		
0X8104	Access not allowed.							
0X8105	D.C					SPPLT.11		
0X8106	D.C					SPPLT.12		
0X8107	D.C					SPPLT.13		

\* Caution 1: ***Clear code***

Character color 0X0 is treated differently inside the ASIC. The ASIC does not change the line memory if the code read in from the character RAM is 0x0 (treated as clear color). Thus no character code can be assigned to character color 0X0. Character color and character code relationship is shown in Table 11.

\* Caution 2:

The value set in this register takes affect immediately.

**Table 11. Color Code and Character Color Relation**

Character Color	Color Code
0X0	-
0X1	<i>SPPLT.01</i>
0X2	<i>SPPLT.02</i>
0X3	<i>SPPLT.03</i>
0X0	-
0X1	<i>SPPLT.11</i>
0X2	<i>SPPLT.12</i>
0X3	<i>SPPLT.13</i>

**Table 12. Parameters and Definitions**

<i>SPPLT.0n</i>	
Palette code 0, Color code n	Color code set for palette 0.
<i>SPPLT.1n</i>	
Palette code 1, Color code n	Color code set for palette 1.
<i>D.C</i>	
Do not care	This register value has no effect.

<sup>16</sup> LUT Look.Up.Table

### 3-7-1. Color Change and Bit Weight

LSB of the data will always be in D0 and its bit weight is the lowest. Screen output is similar with the smallest contrast change being the LSB and the largest the MSB. (Rear most screen has the lightest color.

**Table 13. MSB and LSB Definition**

MSB	LSB
D2	D0

### 3-7-1. Palette LUT for Scroll Plane 1

Palette code (P.C) defined in the scroll plane 1 VRAM (0X9000 0X97FF) is changed to the value set in this register. Register format is as follows.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0X8108	Access not allowed.							
0X8109	D.C					SCIPLT.01		
0X810A	D.C					SCIPLT.02		
0X810B	D.C					SCIPLT.03		
0X810C	Access not allowed.							
0X810D	D.C					SCIPLT.11		
0X810E	D.C					SCIPLT.12		
0X810F	D.C					SCIPLT.13		

\* Caution:

The value set in this register takes effect immediately.

**Table 14. Parameters and Definitions**

<b><i>SCIPLT.0n</i></b>	
Palette code 0, Color code n	Color code set for palette 0.
<b><i>SCIPLT.1n</i></b>	
Palette code 1, Color code n	Color code set for palette 1.
<b><i>D.C</i></b>	
Do not care	This register value has no effect.

### 3-7-3. Palette LUT for Scroll Plane 2

Palette code (P.C) defined in the scroll plane 2 VRAM (0X9800 ~ 0X9FFF) is changed to the value set in this register. Register format is as follows.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0X8110	Access not allowed.							
0X8111	D.C					SC2PLT.01		
0X8112	D.C					SC2PLT.02		
0X8113	D.C					SC2PLT.03		
0X8114	Access not allowed.							
0X8115	D.C					SC2PLT.11		
0X8116	D.C					SC2PLT.12		
0X8117	D.C					SC2PLT.13		

\* Caution:

The value set in this register takes effect immediately.

**Table 15. Parameters and Definitions**

<b>SC2PLT.0n</b>	
Palette code 0, Color code n	Color code set for palette 0.
<b>SC2PLT.1n</b>	
Palette code 1, Color code n	Color code set for palette 1.
<b>D.C</b>	
Do not care	This register value has no effect.

### 3-8. LED CONTROL REGISTER

Register format is as follows.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0X8400	LEDON					Always "1"		

\* Caution:

The value set in this register takes effect immediately.

**Table 16. Parameters and Definitions**

LEDON							
LED control	Sets the flashing property of the indicator LED. D0 ~ D2 is set to a constant "1" to avoid LED from going off due to a program crash.						
	<table><tr><th>Value of LEDON</th><th>Operation</th></tr><tr><td>0X07 ~ 0XFE</td><td>LED Flash: LED flashes with (register value x 10.6[mS]) apart. Flash cycle is set in 3-9. register to set flash cycle.</td></tr><tr><td>0XFF</td><td>LED On: After system reset this is the initial value.</td></tr></table>	Value of LEDON	Operation	0X07 ~ 0XFE	LED Flash: LED flashes with (register value x 10.6[mS]) apart. Flash cycle is set in 3-9. register to set flash cycle.	0XFF	LED On: After system reset this is the initial value.
	Value of LEDON	Operation					
0X07 ~ 0XFE	LED Flash: LED flashes with (register value x 10.6[mS]) apart. Flash cycle is set in 3-9. register to set flash cycle.						
0XFF	LED On: After system reset this is the initial value.						

### 3-9. REGISTERT O SET LED FLASH CYCLE

Register format is shown below.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0X8402	<i>LEDFRQ</i>							

\* Caution:

The value set in this register takes effect immediately.

**Table 17. Parameters and Definition**

<i>LEDFRQ</i>	
LED flash cycle setting	Sets the LED flash cycle. The flash cycle is set with 10.6[ <i>mS</i> ] as the unit time. After system reset the value is 0X80(1.3[ <i>S</i> ]).(initial value)

### 3-10. 2D CIRCUIT RESET REGISTER

This register can be used to reset K1GE. The register format is shown below.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0X87E0	<i>RESET</i>							

\* Caution 1:

The value set in this register takes effect immediately.

**Table 18. Parameters and Definition**

<i>RESET</i>				
2D circuit reset				
	<table> <tr> <th>RESET value</th><th>Operation</th></tr> <tr> <td>0X52</td><td>2D circuit is reset. Value other than 0X52 is ignored.</td></tr> </table>	RESET value	Operation	0X52
RESET value	Operation			
0X52	2D circuit is reset. Value other than 0X52 is ignored.			

\* Caution 2:

All register settings are set to the initialization values when this register is used.

### 3-11. INPUT PORT REGISTER (RESERVED)

Register to read input port (reserved).

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0X87FE	0	INP0	1	1	1	1	1	1

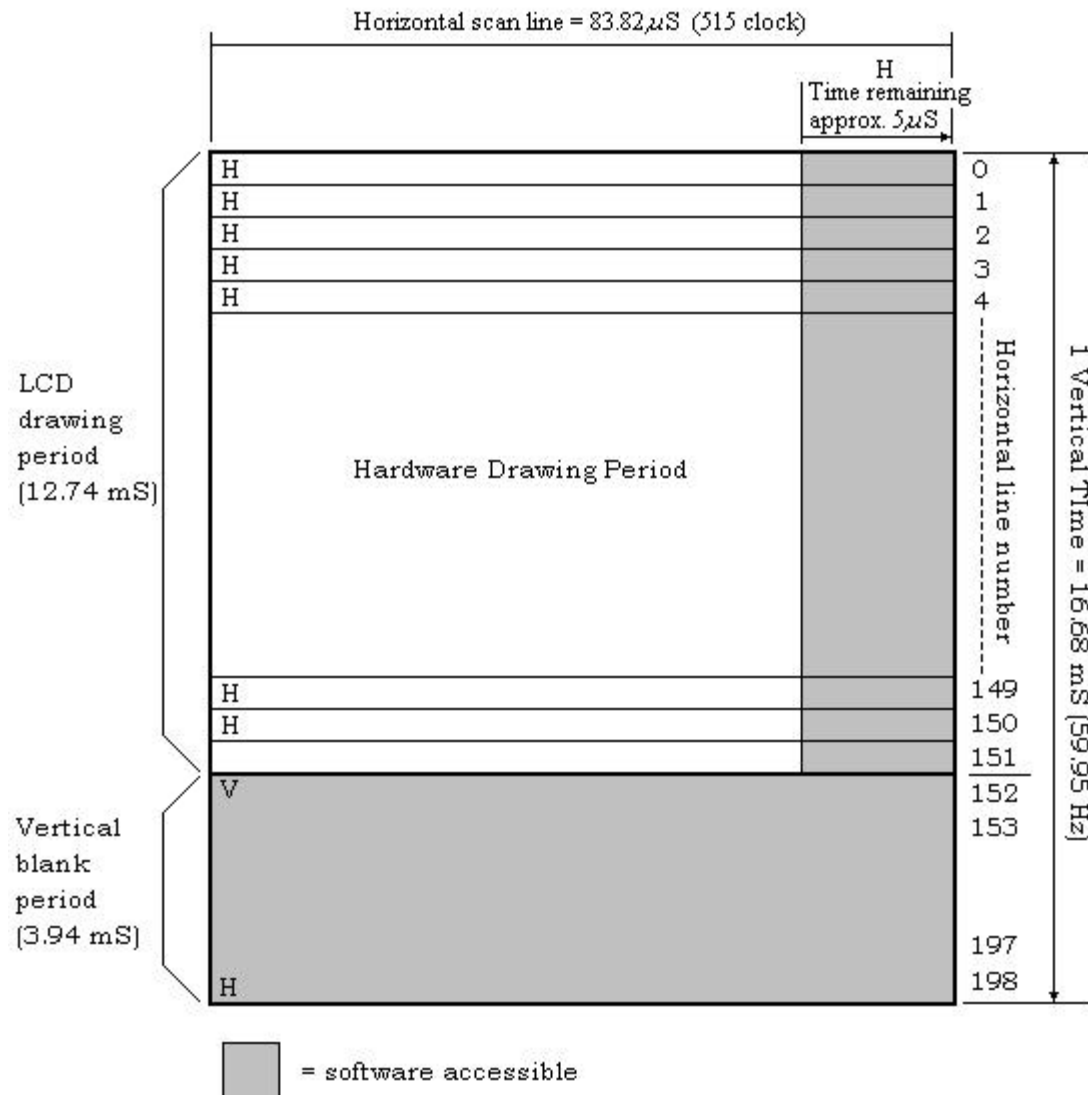
**Table 19. Parameters and Definitions**

INP0							
Input port read	Reserved input port status is read.						
	<table><tr><th>INP0 Logic</th><th></th></tr><tr><td>0</td><td>INP0 = 0 (LO)</td></tr><tr><td>1</td><td>INP1 = 1(HI)</td></tr></table>	INP0 Logic		0	INP0 = 0 (LO)	1	INP1 = 1(HI)
	INP0 Logic						
0	INP0 = 0 (LO)						
1	INP1 = 1(HI)						



## 4. OPERATION TIMING FIGURE

K1GE operation timing is shown below.



\*Access to each RAM area is possible during the Hardware Drawing Period. Please be aware of the adjustment circuitry delaying the Hardware Drawing Period if software accesses the RAM during this period. If the total time surpasses "H Time Remaining (approx. 5 μS)," Character Over occurs. (Accessing the registers does not have an effect. Sprite VRAM, scroll VRAM, and character RAM read/write access invokes the adjustment circuitry.

H = H\_INT generation timing

\*The signal generation begins 1 H before the Hardware Drawing Period starts. (Please be aware H\_INT signal is not generated at line 151 and signal generation for the 0<sup>th</sup> line occurs at the beginning of line 198.)

V = V\_INT generation timing

## 5. REGISTER LAYOUT TABLE

K1GE register layout is shown in the following table.